

# 8.6 A 2.2 $\mu$ W 94nV/√Hz, Chopper-Stabilized Instrumentation Amplifier for EEG Detection in Chronic Implants

Timothy Denison<sup>1</sup>, Kelly Consoer<sup>2</sup>, Andy Kelly<sup>2</sup>, April Hachenburg<sup>2</sup>, Wes Santa<sup>1</sup>

<sup>1</sup>Medtronic Neurological Technology, Columbia Heights, MN

<sup>2</sup>Medtronic Concepts Engineering, Tempe, AZ

Signals for diagnosing chronic disease are often found at low frequencies, leaving instrumentation susceptible to  $1/f$  noise. Excess noise can artificially depress sensitivity or lead to the wrong diagnostic conclusion.

Circuit techniques exist to address excess noise, but are a challenge in low-power design [1]. Chopper stabilization is effective, and has been used in applications for biomedical instrumentation [2,3,4], but at low power the finite bandwidth of choppers creates significant signal distortion. Referring to Fig. 8.6.1, the excess settling time creates even harmonics that lead to distortion and sensitivity errors. Techniques to eliminate distortion have been pursued [3,5], but result in excess quiescent current and complexity in the signal path. Another problem is the limited headroom from the amplified offset prior to chopping and lowpass filtering. Low headroom can artificially limit the front-end gain in low-voltage amplifiers, and undermine performance by adding second-stage noise. These limitations have prevented the application of chopper-stabilized circuits for chronic instrumentation operating from a battery.

The chopper architecture presented here circumvents issues of distortion and limited headroom. The goal is to eliminate the dynamic limitations of chopper stabilization through a combination of AC feedback and chopping at low-impedance nodes. Figure 8.6.2 illustrates the concept in the time domain; after an input step, the up-modulated error signal passes through the stabilized transconductor and is integrated. The integrated output is up-modulated and fed back through a scaled shunt path. Since all chopping is done at low-impedance nodes and the integration is at baseband, the settling requirements are relaxed and second-harmonic distortion is suppressed. A key difference between this design and [2] is that the careful partitioning of modulating circuits in the signal path eliminates the need for output S/Hs to mitigate distortion. The sensitivity error  $\epsilon$  is set by differences in the settling time-constants in the input and feedback paths,  $\epsilon = [T - \tau_{in}]/[T - \tau_{fb}]$ , where  $T$  is the clock period, and  $\tau_{in}$  and  $\tau_{fb}$  are the settling times of the input and feedback switching paths. Scaling the chopping frequency and/or balancing the settling times suppresses second harmonics to insignificant levels. In addition, the servo loop also allows for larger front-end gain by decreasing the headroom requirements for offset. At the output, the AC offset signal is  $\pi f_{3db} A_o V_{off}/(2f_{chop})$ , where  $f_{3db}$  is the lowpass corner of the feedback loop,  $A_o$  is the net gain, and  $f_{chop}$  is the chopping frequency. Offset filtering allows more gain to be placed in the front-end amplifier, which suppresses 2nd-stage noise sources and allows lower supply voltages to be used.

The core element in this scheme is the chopper stabilized differential amplifier, which must modulate signals at low-impedance nodes. This constraint is achieved by modifying a folded-cascode amplifier [3]. Using a folded cascode allows the currents to be partitioned to maximize noise efficiency factor (NEF) [6]. Referring to Fig. 8.6.3, the classical architecture requires only two additional sets of switches: the first set at the source of  $M_{cascode}$  demodulates the AC signal at the input of the amplifier and up-modulates front-end offsets, while the second set is embedded within the self-biased cascode to up-modulate the errors from  $M8/M9$ . Source degeneration of  $M6/M7$  attenuates their offsets. The output of the transconductance stage is at baseband, allowing the integrator to stabilize the feedback loop and filter up-modulated offsets. Suitable input and feedback structures are added to the core amplifier to achieve the desired signal processing.

The target application for the chopper amplifier is an implantable EEG amplifier, which benefits from reduced  $1/f$  noise. To be suit-

able for implantation, the amplifier must provide moderate gain and have low noise (especially  $1/f$  and popcorn noise) while drawing roughly  $1\mu A$  of current from a 1.8V supply. Another goal was to integrate an accurate 0.5Hz high-pass filter monolithically to filter out electrode offsets. An amplifier meeting these requirements can serve as a sensor for enhancing deep brain stimulation therapies. Figure 8.6.4 provides a signal flow diagram and schematic of the prototype design. Since the signals to be passed are up-modulated, poly-poly capacitors can be used to set the gain and filter corners. This is a significant advantage over other designs [2,4], which require on-chip resistors. Differential-to-single-ended conversion is achieved in the first stage with appropriate switch phasing. The lack of symmetry in the first stage does undermine the ultimate CMRR somewhat, however, for an implantable circuit, saline shields the device and this is an acceptable trade-off for power savings. A secondary feedback path provides the high-pass corner. The scaling of the feedback capacitors and the time-constant of the switched-capacitor integrator set the effective high-pass corner accurately without trim. Sampling for the high-pass loop is at the output to minimize aliasing.

The trade-off for this instrumentation amplifier is the finite input impedance and the limited polarization headroom allowed by the high-pass feedback network. These problems are mitigated by the use of small input capacitors (16pF). With a 4kHz chopper clock, the input has an effective differential resistance of 7.5M $\Omega$ , which is high enough to avoid signal attenuation or corrosion with industry-standard Pt-Ir electrodes. The polarization headroom is a trade-off with die area. The standard deviation of Pt-Ir deep brain stimulation electrodes was measured to be 5mV, indicating that a 50mV polarization headroom is acceptable in a chronic amplifier system.

The instrumentation amplifier was prototyped in a 0.8 $\mu$ m CMOS process as part of a brain interface IC, shown in Fig. 8.6.7, and was found to have several key advantages [2-6]. Referring to Fig. 8.6.5, the key benefits include an accurate monolithic high-pass corner, and low noise while operating from a single battery. The low NEF results from the core amplifier cell that eliminates the majority of  $1/f$  noise and distributes currents efficiently, and the ability to put all gain in the front end to eliminate second-stage contributions. Other authors have explored passband feedback in chopper amplifiers, but their implementation is not suitable for implants, requiring 3 orders-of-magnitude more power for a similar noise floor [4]. Designs have been proposed with lower supply, but have more  $1/f$  noise and limited AC CM range [7]. The best NEF in an EEG amplifier published [6], achieves that figure at the expense of higher  $V_{dsat}$  voltages that make single-battery operation difficult. The trade-off of a modest reduction in CMRR compared to [2,4] is not a practical limitation for implantable circuits, where the shielding provided by the body's saline environment significantly attenuates common-mode disturbances like 60Hz.

This work demonstrates an amplifier suitable for monitoring EEG in chronic implants. The concept, however, applies to general asynchronous demodulation and is useful for micropower impedance monitors, accelerometers and pressure sensors. Figure 8.6.6 demonstrates the amplifier's functionality by detecting alpha waves in the EEG over the visual cortex.

## References:

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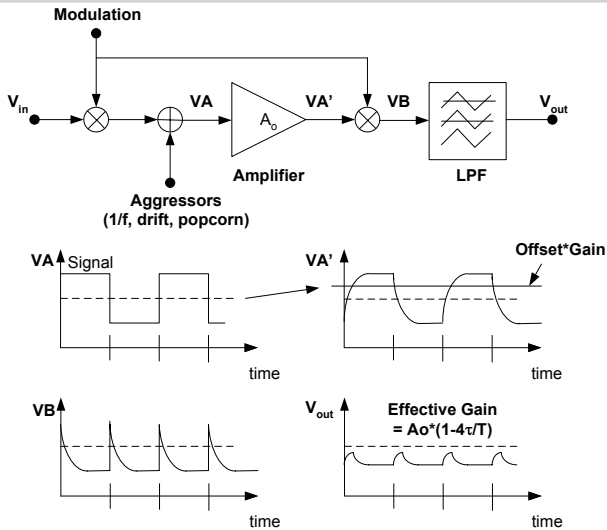


Figure 8.6.1: Distortion and headroom problems encountered with a low-power classical chopper architecture.

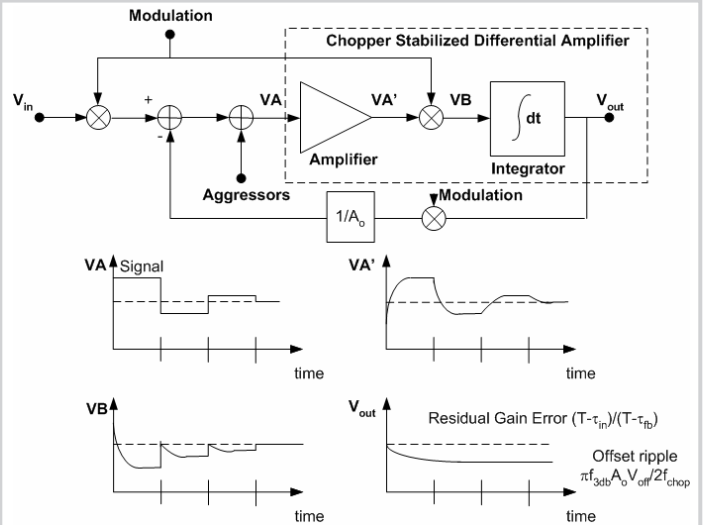


Figure 8.6.2: Feedback of up-modulated signal suppresses distortion and increases headroom.

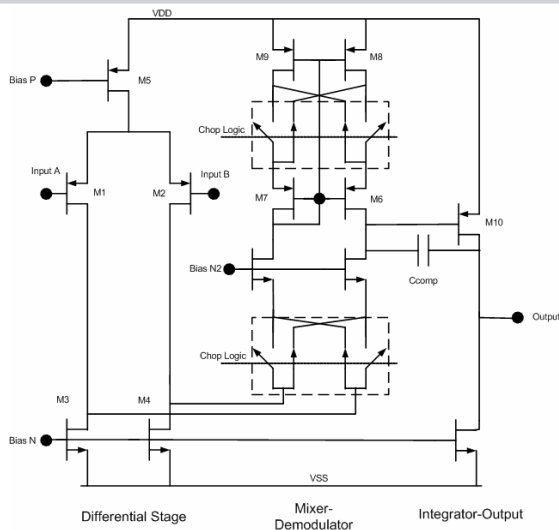


Figure 8.6.3: Modified folded-cascode amplifier that forms the core of the chopper stabilized amplifier.

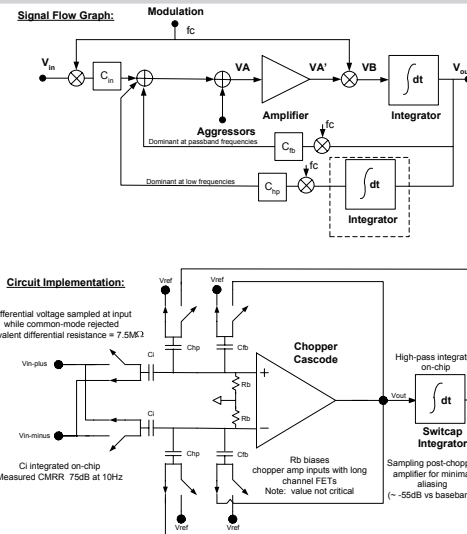


Figure 8.6.4: Signal flow graph and circuit implementation of an instrumentation amplifier suitable for implantable EEG recordings.

PARAMETER	Implant Reqmt	This Work	[2]	[6]	[4]
Supply Current Consumption	<1.5uA	1.2uA	485uA	180nA	20uA
Supply (V)	2.0	1.8	+/-1.5	+/-2.5	3V
NEF	---	4.9	59	4.8	7.8
Gain @ 10Hz	40dB	45.5dB	80dB	39.8dB	>60dB
Input Referred Noise (.5-100 Hz) RMS	1.5uV	0.93uV** (100Hz)	.86uV (150Hz)	1.6uV (30Hz)	0.45uV (40Hz)
CMRR (50/60Hz)	50	105dB	117	>86dB	>110dB
High Pass -3dB frequency	0.5Hz	0.5Hz	0.3Hz*	.014	0.5Hz*
Low Pass -3dB frequency (Trimmed)	150**	250	150	30	>150

\*High-pass filter requires at least one external component/channel.  
 \*\*Equivalent -3dB point of 64Hz, to match NEF definition in [6].

Figure 8.6.5: Summary of results for EEG instrumentation amplifier and comparison to state-of-the-art.

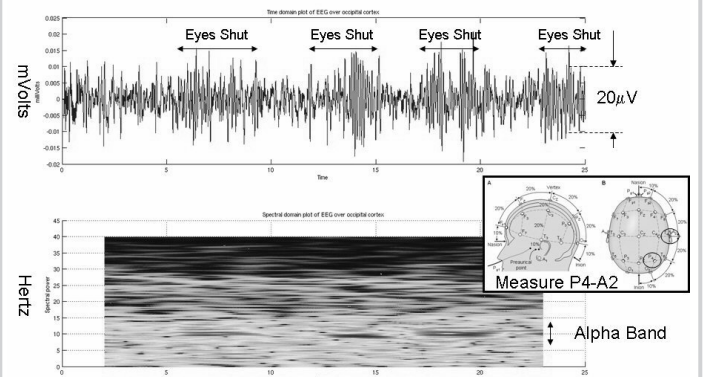


Figure 8.6.6: Demonstration of alpha-wave recognition in the occipital cortex, taken with surface electrodes. When eyes are closed, alpha wave activity yields energy in the spectrogram between 8 and 13Hz.

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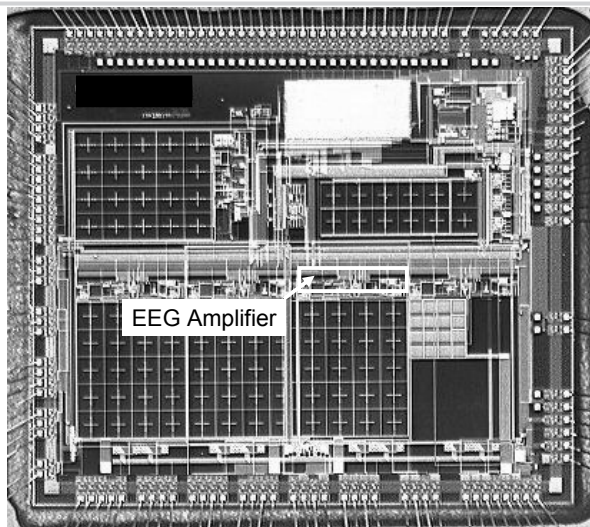


Figure 8.6.7: Die micrograph of biopotential sensing chip. One channel is highlighted.